Oğuz Ergin

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1 EDUCATION

- **Doctor of Philosophy (PhD)** Computer Science, **Binghamton University**, New York, USA May 2005
  Ph.D. Dissertation Title: "Register File Optimizations for Superscalar Microprocessors", Ph.D. Advisor: Prof. Kanad Ghose
- **Master of Science (MS)** Computer Science, **Binghamton University**, New York, USA May 2003
  M.S Thesis Title: "Circuit Techniques for Power-Aware Microprocessors", M.S. Advisor: Prof. Kanad Ghose
- **Bachelor of Science (BS)** Electrical and Electronics Engineering, **Middle East Technical University**, Ankara, Turkey June 2000

2 EMPLOYMENT HISTORY

2.1 Academic History

- **TOBB University of Economics and Technology**, Ankara, Turkey
  - **Office of the Chairman of the Board**
    - **Chief Adviser to the Chairman of the Board** (November'20 – current)
  - **Rector's Office**
    - **Adviser to the Rector - Strategic Planning** (January'15 – current)
      (April'13 – August'13)
  - **Department of Computer Engineering**
    - **Department Chair** (July'16 – current)
    - **Professor** (January'18 – current)
    - **Associate Professor** (April'12 – January'18)
    - **Coordinator of Double Major and Minor Programs** (June'08 – June'12)
    - **Assistant Professor** (June'06 – April'12)
    - **Lecturer** (December'05 – June'06)
  - **Department of Artificial Intelligence Engineering**
    - **Department Chair** (July'19 – August'20)
  - **School of Engineering**
    - **Advisory Board Member of Mechatronics Minor Program** (April'13 – current)
    - **Representative of Assistant Professors in the Faculty Commission** (July'08 – August'11)
  - **Graduate School of Science and Engineering**
    - **Associate Dean** (December'11 – July'13)
  - **Commission Duty**
    - **Chair of the Admissions Commission (Double Major, Minor and Transfer)** (March'17 – current)
    - **Member of the University Processes Commission** (November'10 – September'11)
    - **Member of the Cooperative Education Commission** (October'09 – June'10)
  - **Software Development Coordinator** (August'07 – May'08)
- **Turkish Military Academy**, Ankara, Turkey
  - **Department of Computer Engineering**
    - **Adjunct Professor** (September'17 – January'18)
      (October'15 – January'16)
- **University of Edinburgh**, Edinburgh, UK
  - **School of Informatics - Institute for Computing Systems Architecture**
    - **Research Associate** (May'15 – August'16)
- **University of Notre Dame**, Indiana, USA
  - **Department of Computer Science and Engineering**
    - **Visiting Associate Professor** (January'14 – December'14)
- **State University of New York (SUNY) - Binghamton**, New York, USA
  - **Department of Computer Science and Engineering**
    - **Research Assistant** (June'01 – August'04)
    - **Teaching Assistant** (January'01 – June'04)
      - CS210 – Logic Design
      - CS325 – Computer Organization and Design
      - CS522 – Computer Architecture and Organization

2.2 Industry History

- **Global Supercomputing Corporation,** Eskişehir, Turkey
  - **Consultant and Hardware Design Team Lead** (October'07 – January'09)
- **Intel Barcelona Research Center (IBRC)**, Barcelona, Spain
  - **Senior Research Scientist** (September'04 – November'05)
- **ASELSAN (Military Electronics Industries)**, Ankara, Turkey
  - **Intern,** Thermal Camera Development Group (August'99 – September'99)
- **TAI (Turkish Aerospace Industries)**, Ankara, Turkey

- **Consultant,** R&D Department Avionics Group (June'19 – current)
- **Intern,** R&D Department Avionics Group (August'98 – September'98)

2.3 Entrepreneurship History

- **Kasırga Information Systems Ltd.,** Ankara, Turkey
  - **Founder and CEO** (January'09 – August'17)
    - Supported by the Small and Medium Enterprises Development Organization (KOSGEB) (10.000 TL support from the Turkish government)
- **Yumruk Space and Defense Ltd.,** Ankara, Turkey
  - **Founder and CEO** (March'10 – May'15)
    - Supported by the Turkish Ministry of Industry (100.000 TL for the first year)

3 PUBLICATIONS

3.1 Summary

Type	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	Pending	Total
Book						1																	1
Conference	1	5	4	3	2	1		1	3	2	3	2	2	2	3	2	1		2	1	3		43
Journal		1	3	1	4	1	1	5	1			1	4		2	1	2			1	1		29
Local					1		2						2			2		6					13
Other													1										1
Patent								2		1	2						1			2	1	2	11
Workshop			1		1	1	1	1					1	2				1	1				10
Total	1	6	8	4	8	4	4	9	4	3	5	3	10	4	5	5	4	7	3	4	5	2	108

3.2 Book

1. "Java: Bilgisayar Programlamaya Giriş" [In Turkish; Title means: "Java: Introduction to Computer Programming"]
Ali Yazıcı, Erdoğan Doğdu, A. Murat Özbayoğlu, Y. Murat Erten, **Oğuz Ergin**
Palme Yayıncılık, 2007. ISBN: 978–9944–341–57–8.

3.3 Journal Publications

1. "Can We Trust Undervolting in FPGA-based Deep Learning Designs in Harsh Conditions?"
Fahrettin Koç, Behzad Salami, **Oğuz Ergin**, Osman S. Ünsal, Adrian Kristal
IEEE Micro Magazine **(MICRO)**, to appear.

2. "MoRS: An Approximate Fault Modelling Framework for Reduced-Voltage SRAMs"
İsmail Emir Yüksel, Behzad Salami, **Oğuz Ergin**, Osman S. Ünsal, Adrian Kristal
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **(TCAD)**, October 2021, early access.

3. "Opcode Vector: an Efficient Scheme to Detect Soft Errors in Instructions"
Jorge Martinez, Mert Atamaner, Pedro reviriego, **Oğuz Ergin**, Marco Ottavi
Elsevier Microelectronics Reliability, Vol.86, July 2018, pp.92-97.

4. "GRIM-Filter: fast seed location filtering in DNA read mapping using processing-in-memory technologies"
Jeremie Kim, Damla Şenol Çalı, Honyi Xin, Donghyuk Lee, Saugata Ghose, Mohammed Alser, Hasan Hassan, **Oğuz Ergin**, Can Alkan, Onur Mutlu
BMC Genomics, Vol.19, Sup.2, Article 89, May 2018.

5. "GateKeeper: a new hardware architecture for accelerating pre-alignment in DNA short read mapping"
Mohammed Alser, Hasan Hassan, Hongyi Xin, **Oğuz Ergin**, Onur Mutlu, Can Alkan
Bioinformatics, Vol.33, Issue 21, November 2017, pp.3355-3363.

6. "URFA: Update Based Register File Architecture with Partial Register Write for Energy Efficiency"
Abdulaziz Eker, Yakup Murat Mert, **Oğuz Ergin**
Elsevier Microprocessors and Microsystems **(MICPRO)**, Vol.47, Part B, November 2016, pp.445-453.

7. "Exploiting Existing Copies in Register File for Soft Error Correction"
Abdulaziz Eker, **Oğuz Ergin**
IEEE Computer Architecture Letters **(CAL)**, Vol.15, No.1, January-June 2016, pp.17-20.

8. "Exploiting Existing Comparators for Fine-Grained Low-Cost Error Detection"
Gülay Yalçın, **Oğuz Ergin**, Emrah İşlek, Osman S. Ünsal, Adrian Cristal
ACM Transactions on Architecture and Code Optimization **(TACO)**, Vol.11, No.3, October 2014, Article No. 32.

9. "Bit Impact Factor: Towards Making Fair Vulnerability Comparison"
Serdar Zafer Can, Gülay Yalçın, **Oğuz Ergin**, Osman S. Ünsal, Adrian Cristal
Elsevier Microprocessors and Microsystems **(MICPRO)**, Vol.38, No. 6, August 2014, pp.598-604.

10. "Exploiting Processor Features to Implement Error Detection in Reduced Precision Matrix Multiplications"
Pedro Reviriego, Serdar Zafer Can, Çağrı Eryılmaz, Juan Antonio Maestro, **Oğuz Ergin**
Elsevier Microprocessors and Microsystems **(MICPRO)**, Vol.38, No. 6, August 2014, pp.581-684.

11. "Exploiting Virtual Addressing for Increasing Reliability"
Yaman Çakmakçı, **Oğuz Ergin**
IEEE Computer Architecture Letters **(CAL)**, Vol.13, No.1, January-June 2014, pp.29-32.

12. "Enhanced Duplication: a Technique to Correct Soft Errors in Narrow Values"
İbrahim Burak Karslı, Pedro Reviriego, Muhammed Fatih Ballı, **Oğuz Ergin**, Juan Antonio Maestro
IEEE Computer Architecture Letters **(CAL)**, Vol.12, No.1, January-June 2013, pp.13-16.

13. "Reducing the Energy Dissipation of the Issue Queue by Exploiting Narrow Immediate Operands"
İlknur Cansu Kaynak, Yusuf Onur Koçberber, **Oğuz Ergin**
Journal of Circuits, Systems and Computers **(JCSC)**, Vol. 19, No. 8, December 2010.

14. "Energy-Efficient Register Caching with Compiler Assistance"
Timothy Jones, Michael O'Boyle, Jaume Abella, Antonio González, **Oğuz Ergin**
ACM Transactions on Architecture and Code Optimization **(TACO)**, Vol. 6, Issue 4, Article No. 13, October 2009.

15. "Exploiting Narrow Values for Faster Parity Generation"
Yusuf Onur Koçberber, Yusuf Osmanlıoğlu, **Oğuz Ergin**
Microelectronics International, Vol. 26, Issue 3, 2009, pp.22-29.

16. "Modifying Data-Holding Components of the Processors for Energy Efficiency"
Yusuf Osmanlıoğlu, Yusuf Sinan Hanay, **Oğuz Ergin**
Journal of Circuits, Systems and Computers **(JCSC)**, Vol.18, No.6, October 2009.

17. "Exploring the Limits of Early Register Release: Exploiting Compiler Analysis"
Timothy Jones, Michael O'Boyle, Jaume Abella, Antonio González, **Oğuz Ergin**
ACM Transactions on Architecture and Code Optimization **(TACO)**, Vol. 6, Issue 3, Article No. 12, September 2009.

18. "Reducing Soft Errors through Operand Width Aware Policies"
Oğuz Ergin, Osman S. Ünsal, Xavier Vera, Antonio González
IEEE Transactions on Dependable and Secure Computing **(TDSC)**, Vol. 6, No. 3, July/September 2009, pp.217-230.

19. "Refueling: Preventing Wire Degradation due to Electromigration"
Jaume Abella, Xavier Vera, Osman S. Ünsal, **Oğuz Ergin**, Antonio González, James W. Tschanz
IEEE Micro Magazine **(MICRO)**, Vol. 28, No. 6, November/December 2008, pp.37-46.

20. "Using Tag-Match Comparators for Detecting Soft Errors"
Gülay Yalçın, **Oğuz Ergin**
IEEE Computer Architecture Letters **(CAL)**, Vol. 6, Issue 2, October 2007, pp.53-56.

21. "Impact of Parameter Variations on Circuits and Microarchitecture"
Osman S. Ünsal, James W. Tschanz, Keith Bowman, Vivek De, Xavier Vera, Antonio González, **Oğuz Ergin**
IEEE Micro Magazine **(MICRO)**, Vol. 26, No. 6, November/December 2006, pp.30-39.

22. "Early Register Deallocation Mechanisms Using Checkpointed Register Files"
Oğuz Ergin, Deniz Balkan, Dmitry Ponomarev, Kanad Ghose
IEEE Transactions on Computers **(TC)**, Vol. 55, No. 9, September 2006, pp.1153-1166.

23. "Exploiting Narrow Values for Soft Error Tolerance"
Oğuz Ergin, Osman S. Ünsal, Xavier Vera, Antonio González
IEEE Computer Architecture Letters **(CAL)**, Vol. 5, Issue 2, June 2006.

24. "Instruction Packing: Towards Fast and Energy Efficient Instruction Scheduling"
Joseph Sharkey, Dmitry Ponomarev, Kanad Ghose, **Oğuz Ergin**
ACM Transactions on Architecture and Code Optimization **(TACO)**, Vol. 2, Issue 3, June 2006, pp.156-181.

25. "Reducing the Power Dissipation of Register Alias Tables in High-Performance Processors"
Gürhan Küçük, **Oğuz Ergin**, Dmitry Ponomarev, Kanad Ghose
IEE Proceedings on Computers and Digital Techniques **(PCDT)**, Vol. 152, Issue 6, November 2005, pp.739-746.

26. "Energy-Efficient Comparators for Superscalar Datapaths"
Dmitry Ponomarev, Gürhan Küçük, **Oğuz Ergin**, Kanad Ghose
IEEE Transactions on Computers **(TC)**, Vol. 53, No. 7, July 2004, pp.892-904.

27. "Isolating Short-Lived Operands for Energy Reduction"
Dmitry Ponomarev, Gürhan Küçük, **Oğuz Ergin**, Kanad Ghose
IEEE Transactions on Computers **(TC)**, Vol. 53, No. 6, June 2004, pp.697-709.

28. "Complexity-Effective Reorder Buffer Designs for Superscalar Processors"
Gürhan Küçük, Dmitry Ponomarev, **Oğuz Ergin**, Kanad Ghose
IEEE Transactions on Computers **(TC)**, Vol. 53, No. 6, June 2004, pp.653-665.

29. "Energy-Efficient Issue Queue Design"
Dmitry Ponomarev, Gürhan Küçük, **Oğuz Ergin**, Kanad Ghose, Peter Kogge
IEEE Transactions on Very Large Scale Integration (VLSI) Systems **(TVLSI)**, Vol. 11, No 5, October 2003, pp.789-800.

3.4 Conference and Workshop Publications

1. "ERIC: An Efficient and Practical Software Obfuscation Framework"
Alperen Bolat, Seyid Hikmet Çelik, Ataberk Olgun, **Oğuz Ergin**, Marco Ottavi
51st IEEE/IFIP International Conference on Dependable Systems and Networks **(DSN'21)**, Baltimore, Maryland, USA, June 2022.

2. "Composable Cachelets: Protecting Enclaves from Cache Side-Channel Attacks"
Daniel Townley, Kerem Arıkan, Yu David Lu, Dmitry Ponomarev, **Oğuz Ergin**
31st USENIX Security Symposium **(USENIX SECURITY'22)**, Boston, MA, USA, August 2022.

3. "DR-STRANGE: End-to-End System Design for DRAM True Random Number Generators"
F. Nisa Bostancı, Ataberk Olgun, Jeremie Kim, Lois Orosa, Hasan Hassan, A. Giray Yağlıkçı, **Oğuz Ergin**, Onur Mutlu
28th IEEE Symposium on High Performance Computer Architecture **(HPCA'22)**, Seoul, South Korea, April 2022.

4. "QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAMs"
Ataberk Olgun, A. Giray Yağlıkçı, Minesh Patel, Jeremi Kim, F. Nisa Bostancı, Haocong Luo, Nandita Vijaykumar, **Oğuz Ergin**, Onur Mutlu
50th ACM/IEEE International Symposium on Computer Architecture **(ISCA'21)**, Worldwide Event (due to Covid-19), June 2021.

5. "VoltNet: A Reduced-voltage FPGA-based Accelerator for Convolutional Neural Networks (CNNs)"
Behzad Salami, Baturay Onural, İsmail Emir Yüksel, Fahrettin Koç, **Oğuz Ergin**, Adrián Cristal, Osman S. Unsal, Hamid Sarbazi-Azad, Onur Mutlu
50th IEEE/IFIP International Conference on Dependable Systems and Networks **(DSN'20)**, Valencia, Spain, July 2020.

6. "A Microprocessor Protection Architecture Against Hardware Trojans in Memories"
Alperen Bolat, Luca Cassano, Pedro Reviriego, **Oğuz Ergin**, Marco Ottavi
15th IEEE International Conference on Design&Technology of Integrated Systems **(DTIS'20)**, Marakesh, Morocco, April 2020.

7. "An in-debth Study of Neural Machine Translation Performance"
Simla Burcu Harma, Mario Drumond, Babak Falsafi, **Oğuz Ergin**
1st Workshop on Machine Learning and High Performance **(ML&HPC'20)**, Lausanne, Switzerland, March 2020.

8. "A Novel FPGA-Based High Throughput Accelerator For Binary Search Trees"
Öykü Melikoğlu, **Oğuz Ergin**, Behzad Salami, Julian Pavon, Osman S. Unsal, Adrián Cristal
19th International Workshop on Exploitation of High Performance Heterogeneous Architectures and Accelerators **(WEHA'19)**, Dublin, Ireland, July 2019.

9. "GRIM-Filter: fast seed location filtering in DNA read mapping using processing-in-memory technologies"
Jeremie Kim, Damla Şenol Çalı, Honyi Xin, Donghyuk Lee, Saugata Ghose, Mohammed Alser, Hasan Hassan, **Oğuz Ergin**, Can Alkan, Onur Mutlu
2nd Accelerator Architecture in Computational Biology and Bioinformatics **(AACBB'19)**, Washington, USA, February 2019.
16th Asia Pacific Bioinformatics Conference **(APBC'18)**, Yokohoma, Japan, January 2018.

10. "Detecting Errors in Instructions with Bloom Filters"
Mert Atamaner, **Oğuz Ergin**, Marco Ottavi, Pedro Reviriego Vasallo
30th IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium **(DFTS'17)**, Cambridge, UK, September 2017.

11. "SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies"
Hasan Hassan, Nandita Vijaykumar, Samira Khan, Saugata Ghose, Kevin Chang, Gennady Pekhimenko, **Oğuz Ergin**, Onur Mutlu
23rd IEEE Symposium on High Performance Computer Architecture **(HPCA'17)**, Austin, Texas, February 2017, pp.241-252.

12. "Error Recovery Through Partial Value Similarity"
Abdulaziz Eker, **Oğuz Ergin**
29th IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium **(DFTS'16)**, Connecticut, USA, September 2016, pp.103-106.

13. "Genome Read In-Memory (GRIM) Filter: Fast Location Filtering in DNA Read Mapping with Emerging Memory Technologies"
Jeremie Kim, Damla Şenol, Honyi Xin, Donghyuk Lee, Mohammed Alser, Hasan Hassan, **Oğuz Ergin**, Can Alkan, Onur Mutlu
20th Annual International Conference on Research in Computational Molecular Biology **(RECOMB'16)** *Poster Session*, Santa Monica, CA, April 2016.

14. "ChargeCache: Reducing DRAM Latency by Exploiting Row Access Locality"
Hasan Hassan, Gennady Pekhimenko, Nandita Vijaykumar, Vivek Seshadri, Donghyuk Lee, **Oğuz Ergin**, Onur Mutlu
22nd IEEE Symposium on High Performance Computer Architecture **(HPCA'16)**, Barcelona, Spain, March 2016, pp.581-593.

15. "Collective Pointing: Protecting Pointer Values Against Soft Errors"
Emrah İşlek, Serdar Zafer Can, **Oğuz Ergin**
5th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale **(MEDIAN'Finale)**, Talinn, Estonia, November 2015, pp.54-59.

16. "Exploiting Existing Replicas of Stack Pointer in Register File for Error Detection"
Hale Oğur, Davut Deniz Yavuz, Gözde Boztepe, Serhat Gesoğlu, Abdulaziz Eker, Gülay Yalçın, Osman S. Ünsal, **Oğuz Ergin**
5th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale **(MEDIAN'Finale)**, Talinn, Estonia, November 2015, pp.60-67.

17. "Using Value Similarity of Registers for Soft Error Mitigation"
Abdulaziz Eker, **Oğuz Ergin**
28th IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium **(DFTS'15)**, Amherst, Massachusetts, USA, October 2015, pp.91-96.

18. "User Specific Skin Temperature-Aware DVFS for Smartphones"
Begüm Birsen Eğilmez, Gökhan Memik, Seda Öğrenci-Memik, **Oğuz Ergin**
18th Design, Automation and Test in Europe **(DATE'15)**, Grenoble, France, March 2015, pp.1217-1220.

19. "Exploiting a Fast and Simple ECC for Scaling Supply Voltage in Level-1 Caches"
Gülay Yalçın, Adrian Cristal, Osman S. Ünsal, **Oğuz Ergin**, Emrah İşlek, Öykü Tozlu, Pedro Reviriego,
20th IEEE International On-Line Testing Symposium **(IOLTS'14)**, Catalunya, Spain, July 2014, pp.1-6.

20. "Improving the Reliability of Skewed Caches through ECC based Hashes"
Sercan Yeğin, İbrahim Burak Karslı, **Oğuz Ergin**, Marco Ottavi, Salvatore Pontarelli, Pedro Reviriego
3rd Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale **(MEDIAN'14)**, Dresden, Germany, March 2014.

21. "GPU Based Parallel Image Processing Library for Embedded Systems"
Mustafa Çavuş, Hakkı Doğaner Sümerkan, Osman Seçkin Şimşek, Hasan Hassan, Abdullah Giray Yağlıkçı, **Oğuz Ergin**
9th International Conference on Computer Vision Theory and Applications **(VISAPP'14)**, Lisbon, Portugal, January 2014, pp.234-241.

22. "Adapting the Columns of Storage Components for Lower Static Energy Dissipation"
Mehmet Burak Aykenar, Muhammet Özgür, Osman Seçkin Şimşek, **Oğuz Ergin**
21st IFIP/IEEE International Conference on Very Large Scale Integration **(VLSI-SoC'13)**, Istanbul, Turkey, October 2013, pp.222-227.

23. "Exploiting Replicated Checkpoints for Soft Error Detection and Correction"
Fahrettin Koç, Kenan Bozdaş, İbrahim Burak Karslı, **Oğuz Ergin**
16th Design, Automation and Test in Europe **(DATE'13)**, Grenoble, France, March 2013, pp.1494-1497.

24. "Exploiting Bus Level and Bit Level Inactivity for Preventing Wire Degradation due To Electromigration"
Mehmet Kayaalp, Fahrettin Koç, **Oğuz Ergin**
15th Euromicro Symposium on Digital System Design **(DSD'12)**, Izmir, Turkey, September 2012.

25. "Improving the Soft Error Resilience of the Register Files Using SRAM Bitcells with Builtin Comparators"
Mehmet Kayaalp, Fahrettin Koç, **Oğuz Ergin**
15th Euromicro Symposium on Digital System Design **(DSD'12)**, Izmir, Turkey, September 2012.

26. "Global Co-op: Engineering Education through Outsourcing"
Oğuz Ergin, Utku Diril, Wei-Jin Dai
2nd Interdisciplinary Engineering Design Education Conference **(IEDEC'12)**, Santa Clara, California, USA, March 2012.

27. "Tag Simplification: Achieving Power Efficiency through Reducing the Complexity of the Wakeup Logic"
Mehmet Burak Aykenar, Muhammet Özgür, Vehbi Eşref Bayraktar, **Oğuz Ergin**
2nd International Conference on Energy Aware Computing **(ICEAC'11)**, Istanbul, Turkey, December 2011.

28. "Using Content-Aware Bitcells to Reduce Static Energy Dissipation"
Fahrettin Koç, Osman Seçkin Şimşek, **Oğuz Ergin**
29th International Conference on Computer Design **(ICCD'11)**, Amherst, Massachusetts, USA, October 2011, pp.51-56.

29. "Dynamic Register File Partitioning in Superscalar Microprocessors for Energy Efficiency"
Meltem Özsoy, Yusuf Onur Koçberber, Mehmet Kayaalp, **Oğuz Ergin**
28th International Conference on Computer Design **(ICCD'10)**, Amsterdam, Netherlands, October 2010, pp.515-520.

30. "Complexity-Effective Rename Table Design for Rapid Speculation Recovery"
Görkem Aşılıoğlu, Emine Merve Kaya, **Oğuz Ergin**
23th Conference on Architecture of Computing Systems **(ARCS'10)**, Hannover, Germany, February 2010, pp.15-24.

31. "Exploiting Inactive Rename Slots for Detecting Soft Errors"
Mehmet Kayaalp, **Oğuz Ergin**, Osman S. Ünsal, Mateo Valero
23th Conference on Architecture of Computing Systems **(ARCS'10)**, Hannover, Germany, February 2010, pp.126-137.

32. "Reducing Parity Generation Latency through Input Value Aware Circuits"
Yusuf Osmanlıoğlu, Yusuf Onur Koçberber, **Oğuz Ergin**
19th ACM Great Lakes Symposium on VLSI **(GLSVLSI'09)**, Boston, Massachusetts, USA, May 2009, pp.109-112.

33. "Exploiting Register Renaming Logic for Soft Error Detection"
Oğuz Ergin, Gülay Yalçın, Osman S. Ünsal, Mateo Valero
1st Workshop on Design for Reliability **(DFR'09)**, Paphos, Southern Cyprus, January 2009.

34. "Evaluating the Effects of Compiler Optimizations on AVF"
Timothy Jones, Michael O'Boyle, **Oğuz Ergin**
12nd Annual Workshop on the Interaction between Compilers and Computer Architecture **(INTERACT'08)**, Salt Lake City, Utah, USA, February 2008.

35. "Fuse: A Technique to Anticipate Failures due to Degradation in ALUs"
Xavier Vera, Jaume Abella, Osman S. Ünsal, **Oğuz Ergin**, Antonio González
13th IEEE International On-Line Testing Symposium **(IOLTS'07)**, Crete, Greece, July 2007.

36. "Designing Efficient Processors Using Compiler-Directed Optimisations"
Timothy Jones, Michael O'Boyle, Jaume Abella, Antonio González, **Oğuz Ergin**
11th Annual Workshop on the Interaction between Compilers and Computer Architecture **(INTERACT'07)**, Phoenix, Arizona, USA, February 2007.

37. "Exploiting Narrow Values for Energy Efficiency in the Register Files of Superscalar Microprocessors"
Oğuz Ergin
16th International Workshop on Power and Timing Modeling, Optimization and Simulation **(PATMOS'06)**
Lecture Notes in Computer Science, (LNCS 4148), Springer-Verlag, 2006, pp.477-485

38. "Empowering a Helper Cluster through Data-Width Aware Instruction Selection Policies"
Osman S. Ünsal, **Oğuz Ergin**, Xavier Vera, Antonio González
International Parallel and Distributed Processing Symposium **(IPDPS'06)**, Rhodes, Greece, April 2006.

39. "Checker Backend for Soft and Timing Error Detection and Recovery"
Xavier Vera, Jaume Abella, Osman S. Ünsal, Antonio González, **Oğuz Ergin**
2nd Workshop on System Effects of Logic Soft Errors **(SELSE 2)**, Urbana-Champaign, Illinois, USA, April 2006.

40. "Power-Efficient Wakeup Tag Broadcast"
Joseph Sharkey, Dmitry Ponomarev, Kanad Ghose, **Oğuz Ergin**
23rd International Conference on Computer Design **(ICCD'05)**, San Jose, USA, October 2005, pp.654-6 61.

41. "Compiler Directed Early Register Release"
Timothy Jones, Michael O'Boyle, Jaume Abella, Antonio González, **Oğuz Ergin**
14th International Conference on Parallel Architectures and Compilation Techniques **(PACT'05)**, Saint Louis, USA, September 2005, pp.110-119.

42. "Instruction Packing: Reducing Power and Delay of the Dynamic Scheduling Logic"
Joseph Sharkey, Dmitry Ponomarev, Kanad Ghose, **Oğuz Ergin**
International Symposium on Low Power Electronics and Design **(ISLPED'05)**, San Diego, USA, August 2005, pp.30-35.

43. "Reducing Delay and Power Consumption of the Wakeup Logic through Instruction Packing and Tag Memoization"
Joseph Sharkey, Dmitry Ponomarev, Kanad Ghose, **Oğuz Ergin**

Workshop on Power Aware Computer Systems **(PACS'04)**
Lecture Notes in Computer Science, (LNCS 3471), Springer-Verlag, 2005, pp.15-29.

44. "Register Packing: Exploiting Narrow-Width Operands for Reducing Register File Pressure"
Oğuz Ergin, Deniz Balkan, Kanad Ghose, Dmitry Ponomarev
37th International Symposium on Microarchitecture **(MICRO'04)**, Portland, USA, December 2004, pp.304-315.

45. "Increasing Processor Performance Through Early Register Release"
Oğuz Ergin, Deniz Balkan, Dmitry Ponomarev, Kanad Ghose
22nd International Conference on Computer Design **(ICCD'04)**, San Jose, USA, October 2004, pp.480-487.

46. "Defining Wakeup Width for Efficient Dynamic Scheduling"
Aneesh Aggarwal, Manoj Franklin, **Oğuz Ergin**
22nd International Conference on Computer Design **(ICCD'04)**, San Jose, USA, October 2004, pp.36-41.

47. "Selective Writeback: Improving Processor Performance and Energy Efficiency"
Deniz Balkan, **Oğuz Ergin**, Dmitry Ponomarev, Kanad Ghose
1st IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers **(P=AC^{2}I'04)**, IBM Research Center, Yorktown Heights, USA, October 2004, pp.171-180.

48. "Distributed Reorder Buffer Schemes for Low Power"
Gürhan Küçük, **Oğuz Ergin**, Dmitry Ponomarev, Kanad Ghose
21st International Conference on Computer Design **(ICCD'03)**, San Jose, USA, October 2003, pp.258-268.

49. "Reducing Datapath Energy Through the Isolation of Short-Lived Operands"
Dmitry Ponomarev, Gürhan Küçük, **Oğuz Ergin**, Kanad Ghose
12th International Conference on Parallel Architectures and Compilation Techniques **(PACT'03)**, New Orleans, USA, September 2003, pp.258-268.

50. "Energy-Efficient Register Renaming"
Gürhan Küçük, **Oğuz Ergin**, Dmitry Ponomarev, Kanad Ghose
Proceedings of *13th International Workshop on Power and Timing Modeling, Optimization and Simulation* **(PATMOS'03)**
Lecture Notes in Computer Science, (LNCS 2799), Springer-Verlag, 2003, pp.219-228.

51. "Power Efficient Comparators for Long Arguments in Superscalar Processors"
Dmitry Ponomarev, Gürhan Küçük, **Oğuz Ergin**, Kanad Ghose
International Symposium on Low Power Electronics and Design **(ISLPED'03)**, Seoul, South Korea, August 2003, pp.378-383.

52. "Reducing Reorder Buffer Complexity Through Selective Operand Caching"
Gürhan Küçük, Dmitry Ponomarev, **Oğuz Ergin**, Kanad Ghose
International Symposium on Low Power Electronics and Design **(ISLPED'03)**, Seoul, South Korea, August 2003, pp.235-240.

53. "A Circuit-Level Implementation of Fast, Energy-Efficient CMOS Comparators for High-Performance Microprocessors"
Oğuz Ergin, Kanad Ghose, Gürhan Küçük, Dmitry Ponomarev
20th International Conference on Computer Design **(ICCD'02)**, Freiburg, Germany, September 2002, pp.118-121.

3.5 Patents

1. "Supply voltage adjustment system and method depending on temperature"
Fulya Ağırnas, Fatih Say, **Oğuz Ergin**
Turkish Patent TR 2019/19973. *filed: December 12, 2019* *pending* *Assignee: ASELSAN*

2. "Adaptable Substone Polaring (Body Bias) A Dynamic Random Access Memory (DRAM) Structure With Voltage"
Oğuz Ergin, Fahrettin Koç
Turkish Patent TR 2019/10444. *filed: July 12, 2019* *pending* *Assignee: TOBB University of Economics and Technology*

3. "A Dynamic Random Access Memory (DRAM) Structure With Adjustable Body Bias Voltage According To The Temperature Limit"
Oğuz Ergin, Fahrettin Koç
Turkish Patent TR 2019/13677. *filed: September, 10, 2019* *granted: January 21, 2022* *Assignee: TOBB University of Economics and Technology*

4. "A Dynamic Random Access Memory (DRAM) structure with body bias voltage that can be adapted to the access pattern of cells"
Oğuz Ergin, Fahrettin Koç
Turkish Patent TR 2019/17243. *filed: November, 7, 2019* *granted: September 4, 2021* *Assignee: TOBB University of Economics and Technology*

5. "One direction-shift register aliasing table circuit suitable for use in microprocessors"
Oğuz Ergin, İlker Polat
Turkish Patent TR 2019/11815. *filed: July 12, 2019* *granted: March 3, 2021* *Assignee: TOBB University of Economics and Technology*

6. "A sensing and reporting system"
Oğuz Ergin
Turkish Patent TR 2015/14556. *filed: November 18, 2015* *granted: July 23, 2018* *Assignee: TOBB University of Economics and Technology*

7. "Dynamically Estimating the Lifetime of Semiconductor Storage Elements"
Xavier Vera, Jaume Abella, Osman S. Ünsal, **Oğuz Ergin**, and Antonio González
US Patent 8,151,094. *filed: December 30, 2005* *granted: April 3, 2012* *Assignee: Intel Corporation*

8. "Detecting Soft Errors via Selective Re-execution"
Xavier Vera, **Oğuz Ergin**, Osman S. Ünsal, Jaume Abella, and Antonio González
US Patent 8,090,996. *filed: March 31, 2006* *granted: January 3, 2012* *Assignee: Intel Corporation*

9. "Enhancing Reliability of a Many-Core Processor"
Xavier Vera, Osman S. Ünsal, **Oğuz Ergin**, Jaume Abella, and Antonio González
US Patent 8,074,110. *filed: February 28, 2006* *granted: December 6, 2011* *Assignee: Intel Corporation*

10. "Clustered Variations-Aware Microarchitecture"
Xavier Vera, **Oğuz Ergin**, Osman S. Ünsal and Antonio González
US Patent 7,600,145. *filed: October 26, 2005* *granted: October 6, 2009* *Assignee: Intel Corporation*

11. "Reducing the Soft Error Vulnerability of Stored Data"
Oğuz Ergin, Osman S. Ünsal, Xavier Vera and Antonio González
US Patent 7,558,992. *filed: October 10, 2005* *granted: July 7, 2009* *Assignee: Intel Corporation*

3.6 Local Publications (in Turkish)

1. "ADRAM: Yenileme Sıklığı İyileştirilmiş Düşük Güç Tüketimli Adaptif DRAM Mimarisi"
["ADRAM: Low Power Adaptive DRAM Architecture through Improved Refresh Rate"]
Fahrettin Koç, Fatma Nisa Bostancı, **Oğuz Ergin**
Processor Design Workshop, İstanbul, Turkey, September 2019.

2. "Yazmaç Öbeğindeki Geçici Hataları Düzeltmek İçin Yükleme-Kaydetme Kuyruğundaki Hazır Kopyaların Kullanılması"
["Using Values Inside Load Store Queue for Error Correction in Register File"]
Buğra Çon, **Oğuz Ergin**
Processor Design Workshop, İstanbul, Turkey, September 2019.

3. "FPGA BRAM'lerde Çalışma Voltajı Düşürülmesine Sıcaklığın Etkileri"
["The Affects of Temperature on Undervolting in FPGA BRAMs"]
Fulya Agirnas, Fatih Say, **Oğuz Ergin**
Processor Design Workshop, İstanbul, Turkey, September 2019.

4. "Süperiletken Bilgisayarlar İçin SRAM Bellek Tasarımı"
["SRAM Memory Design for Superconductor Based Computers"]
İlker Polat, **Oğuz Ergin**, Ali Bozbey
Processor Design Workshop, İstanbul, Turkey, September 2019.

5. "DNN Mikroservisleri ile Makine Çevirisi Modelleri için Performans Analizi"
["An in-depth Study of Neural Machine Translation Performance"]
Simla Harma, Mario Drumond, **Oğuz Ergin**, Babak Falsafi
Processor Design Workshop, İstanbul, Turkey, September 2019.

6. "Donanım Düzeyindeki Truva Atlarının Program Belleğinde Çevrimiçi Belirlenmesi"
["On-line Detection ve Prevention of HW Trojans in Program Memories"]
Alperen Bolat, **Oğuz Ergin**, Marco Ottavi, Luca Cassano, Pedro Reviriego
Processor Design Workshop, İstanbul, Turkey, September 2019.

7. "DRAM Bellek Gecikmelerini azaltabilmek için Yedek Dize Yöntemi"
["Duplicating Frequently Accessed Rows for Reducing DRAM Memory Latency: Copied Row Approach"]
Eyüphan İpek, Hasan Hassan, **Oğuz Ergin**
19th Academic Computing **(AB)**, Aksaray, Turkey, February 2017.

8. "GPU Önbelleklerinde Yerelliğe Bağlı Dinamik Yazma Politikası"
["Locality Driven Dynamic Cache Write Policy on Graphics Processing Units"]
Çağatay Turgut, **Oğuz Ergin**
19th Academic Computing **(AB)**, Aksaray, Turkey, February 2017.

9. "Çok Çekirdekli İşlemciler için Ölçeklenebilir Çok Portlu Yazmaç Öbeğinin FPGA Tasarımı"
["FPGA Implementation of a Scalable Multi-Port Register File for Many-Core Processors"]
A. Giray Yağlıkçı, Hasan Hassan, **Oğuz Ergin**, Fatih Say
4th Turkish National Embedded Systems and Applictions Symposium **(GömSis 2014)**, Istanbul, Turkey, November 2014.

10. "FIR Filtre Uygulamalarını Hızlandırmak: FPGA ve GPU Performans Karşılaştırması"
["FPGA vs GPU Performance Comparison on the Implementation of FIR Filters"]
Mehmet Burak Aykenar, Hasan Hassan, **Oğuz Ergin**
22nd Signal Processing and Communications Applications Conference **(SİU'14)**, Trabzon, Turkey, April 2014.

11. "Verileri Nota Kullanarak Şifreleme ve Ses Dosyası İçerisine Gizleme"
["Encrypting Data Using Musical Notes and Hiding This Information Inside Audio Files"]
Muhammet Hamdi Yavuz, **Oğuz Ergin**
3rd International Conference on Information Security and Cryptology **(ISCTurkey'08)**, Ankara, Turkey, December 2008.

12. "Telsiz Bilgisayar Mimarisi"
["Wireless Computer Architecture"]
Oğuz Ergin, Yusuf Onur Koçberber, Meltem Özsoy
1st Turkish National Embedded Systems and Applictions Symposium **(GömSis 2008)**, Istanbul, Turkey, November 2008, p:2.

13. "Güç Kesintisi Uygulayan Devrelerin Uyanma Gecikmelerinin Belirlenme Zamanının Azaltılması"
["Decreasing the Simulation Time for Calculating the Wakeup Latency of the Circuits That Employ Sleep Transistors"]
Yusuf Sinan Hanay, **Oğuz Ergin**, Utku Diril
Turkish National Meeting on Automatic Control **(TOK'06)**, Ankara, Turkey, November 2006, pp.185-189.

3.7 Other Publications

1. "Why the Names? Anubanini and His Clan in the Cuthaean Legend"
Selim F. Adalı, M. Fatih Demirci, A. Murat Özbayoğlu, **Oğuz Ergin**
Gephyra 11, 2014, pp.15-28.

4 ACADEMIC ACTIVITIES

4.1 Grants

4.1.1 Principle Investigator

1. "Development of a Microprocessor and SoC for Defence and Civil Purposes"
   Kindi, July 2021 – June 2022
   Budget: 408.861 TL for 12 months (4 graduate students, equipment)
2. "Development of a Microprocessor and SoC for Defence and Civil Purposes"
   Rovenma, December 2020 – May 2021
   Budget: 176.583 TL for 6 months (4 graduate students, equipment)
3. "Design and Implementation of the Cache Architecture for Mission-Critical Multicore Microprocessors"
   ASELSAN (Military Electronics Industries) – SAYP Programme, October 2017 – October 2019
   Budget: 74.118 TL for 18 months (1 graduate student, equipment)
4. "Design of a Processor Core of the Turkish National Microprocessor"
   ASELSAN (Military Electronics Industries), October 2017 – October 2019
   Budget: 250.000 TL for 18 months (2 graduate and 2 undergraduate students, equipment)
5. "OpenCL Compatible High Performance Accelerator Hardware Design for AIHS"
   ASELSAN (Military Electronics Industries), May 2013 – April 2015
   Budget: ~180.000 TL for 18 months (4 graduate students, equipment)
6. "Reliable Microprocessor Design"
   The Scientific and Technological Research Council of Turkey (TÜBİTAK) – COST Programme, June 2012 – June 2015.
   Budget: 240.988 TL for 36 months (3 graduate students, travel, equipment)
7. "Development of an OpenCL Based Image Processing Library"
   Turkish Ministry of Science, Industry and Technology – SANTEZ Programme, March 2012 – March 2014.
   Budget: 140.550 TL for 24 months (2 graduate students, travel, equipment)
8. "Design of an Embedded Processor, Designing the Test Infrastructure for OpenCL Driver and Compilers of Vivante Graphical Processors"
   Vivante Corporation, Silicon Valley (USA), May 2011 – June 2012.
   Budget: $108.830 for 14 months (3 graduate and 4 undergraduate students, equipment)
9. "A Scalable Register Renaming Technique"
   The Scientific and Technological Research Council of Turkey (TÜBİTAK) – 1001 Programme, September 2009 – September 2011.
   Budget: 116.450 TL for 24 months (2 graduate students, travel, equipment)
10. "Reducing the power dissipation of out-of-order microprocessors by detecting narrow values and narrow value phases"
    The Scientific and Technological Research Council of Turkey (TÜBİTAK) – 1001 Programme, July 2007 – July 2009.
    Budget: 96.650 TL for 24 months (2 graduate students, travel, equipment)
11. "Reliable Embedded Processors"
    European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC), July 2007 – December 2008.
    Budget: €20.400 for 12 months (1 graduate student, travel)

4.1.2 Co-Principal Investigator

1. "Development of Multi-Module Main IC (M3I) Submodules for Superconducting Integrated Circuits"
   The Scientific and Technological Research Council of Turkey (TÜBİTAK) – 1001, April 2018 – April 2021.
   Principle Investigator: Associate Prof. Ali Bozbey, Budget: 550.000 TL for 36 months

4.1.3 Consultant

2. "Development of an RSFQ Based Integrated Circuit Design Tool and Arithmetic Logic Unit"
   The Scientific and Technological Research Council of Turkey (TÜBİTAK) – 1001, February 2012 – February 2015.
   Principle Investigator: Assistant Prof. Ali Bozbey, Budget: 445.691 TL for 36 months

4.1.4 Management Committee Member

1. "Manufacturable and Dependable Multicore Architectures at Nanoscale"
   European Cooperation in Science and Technology (COST), Information and Communication Technologies (ICT)
   COST Action IC1103, December 2011 – December 2015.

4.2 Courses Taught

- **Turkish Military Academy**, Ankara, Turkey
  - BM 4102 **Computer Architecture** [(Fall: 2015, 2017)]
- **University of Notre Dame**, Notre Dame, Indiana, United States
  - CSE 60321 **Advanced Computer Architecture** [(Spring: 2014)]
  - CSE 60462 **VLSI Design** [(Fall: 2014)]
- **TOBB University of Economics and Technology**, Ankara, Turkey
  - BİL 102 **Programming with Java** [(Spring: 2006)]
  - BİL 264 **Logic Design** [(Fall: 2011 – 2013, 2015, 2017) (Spring: 2007, 2013, 2015) (Summer: 2006, 2015 – 2017)]
  - BİL 264L **Logic Design Laboratory** [(Fall: 2011 – 2013, 2015, 2017) (Spring: 2013, 2015) (Summer: 2006, 2015 – 2017)]
  - BİL 361 **Computer Architecture and Organization**
    [(Fall: 2006 – 2008, 2012, 2013, 2015 - 2021) (Spring: 2010 – 2013, 2015 – 2022) (Summer: 2011, 2013)]
  - BİL 362 **Microprocessors** [(Fall: 2008 – 2010, 2012) (Spring: 2007 – 2009) (Summer: 2009 – 2011)]
  - BİL 362L **Microprocessors Laboratory** [(Fall: 2008 – 2010, 2012) (Spring: 2007 – 2009) (Summer: 2009 – 2011)]

- BİL 465/BİL566 **Advanced Computer Architecture** [(Fall: 2008 – 2010) (Spring: 2012) (Summer: 2009)]
- BİL 466/BİL569 **Embedded Systems** [(Spring: 2011)]
- ELE 222 **Analog Electronics** [(Spring: 2006)]
- ELE 222L **Analog Electronics Laboratory** [(Spring: 2006)]

4.3 Student Advising

4.3.1 Summary (by year of completion)

Type	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	Ongoing	Total
Postdoc						1											1
PhD										1						1	2
MS	3		2	2	2	1	2	5	2	1	2		2	2	2	5	33
Undergraduate			2	2				2	1	1				1	1	1	11
Total	**3**	**-**	**4**	**4**	**2**	**2**	**2**	**7**	**3**	**3**	**2**	**-**	**2**	**3**	**3**	**7**	**47**

4.3.2 Postdoctoral Researcher

- TOBB University of Economics and Technology, Ankara, Turkey

1. Kenan Bozdaş, Nisan 2011 – June 2012. *After postdoc:* ***TÜBİTAK SAGE*** *(R&D Engineer), Ankara, Turkey*

4.3.3 Doctor of Philosophy (Ph.D.)

- TOBB University of Economics and Technology, Ankara, Turkey

1. Abdülaziz Eker, August 2016. *After graduation:* ***TÜBİTAK İLTAREN*** *(R&D Engineer), Ankara, Turkey*
Currently at: ***Philips*** *(R&D Engineer), Eindhoven, Netherlands*
Thesis Title: "Avoiding Register File Inefficiency in Terms of Power and Reliability"

2. Fahrettin Koç, expected graduation in 2022.

4.3.4 Master of Science (M.S.)

- TOBB University of Economics and Technology, Ankara, Turkey

1. Esra Nur Ayaz, December 2021. *After graduation:* ***University of Edinburgh*** *(PhD Student), Edinburgh, Scotland*
Thesis Title: "SONATA: Specialized Address Registers To Reduce Power Consumption"

2. Ataberk Olgun, December 2021. *After graduation:* ***ETH Zurich*** *(PhD Student), Zurich, Switzerland*
Thesis Title: "High Throughput True Random Number Generation Using Quadruple Row Activation in Real DRAM Chips"

3. Mert Atamaner, July 2020. *After graduation:* ***Rovenma*** *(Digital Design Engineer), Ankara, Turkey*
Currently at: ***ASELSAN*** *(Embedded Software Engineer), Ankara, Turkey*
Thesis Title: "Cache Design and Implementation for Mission-Critical Multicore Processors"

4. Simla Burcu Harma, January 2020. *After graduation:* ***Ecole Polytechnique Federale de Lausenne (EPFL)*** *(PhD Student), Switzerland*
Thesis Title: "An In-Depth Performance Analysis of Neural Machine Translation Tasks"

5. Fulya Ağırnas, November 2019. *After graduation:* ***ASELSAN*** *(Digital Design Engineer), Ankara, Turkey*
Thesis Title: "The effects of temperature to Undervolting in terms of Error Rate and Power and a Temperature Controlled Undervolting Method"

6. Öykü Melikoğlu, August 2019. *After graduation:* ***Freelance,*** *Ankara, Turkey*
Thesis Title: "Accelerated High Throughput Parallel Search on Binary Search Trees via Field Programmable Gate Arrays"

7. Çağatay Turgut, August 2017. *After graduation:* ***Meteksan Savunma*** *(R&D Engineer), Ankara, Turkey*
Thesis Title: "Locality Driven Dynamic Cache Write Policy on Graphics Processing Units"

8. Eyüphan İpek, April 2017. *After graduation:* ***SDT*** *(R&D Engineer), Ankara, Turkey*
Currently at: ***TAI*** *(Avinocs Digital Design Engineer), Ankara, Turkey*
Thesis Title: "Hardware Based Accelerator Design for DRAM Operations"

9. Hasan Hassan, August 2016. *After graduation:* ***ETH Zurich*** *(PhD Student), Zurich, Switzerland*
Thesis Title: "Reducing DRAM Access Latency by Exploiting DRAM Leakage Characteristics and Common Access Patterns"

10. Serdar Zafer Can, August 2015. *After graduation:* ***University of Minnesota*** *(PhD Student), Minneapolis, USA*
Currently at: ***TAI*** *(R&D Engineer), Ankara, Turkey*
Thesis Title: "Bit Impact Factor: Towards Making Fair Vulnerability Comparison"

11. Emrah İşlek, May 2015. *After graduation:* ***RST Technologies*** *(R&D Engineer), Ankara, Turkey*
Currently at: ***Havelsan*** *(Software Engineer), Ankara, Turkey*
Thesis Title: "Collective Pointing: Protecting Pointer Values Against Soft Errors on Processors"

12. Muhammet Özgür, December 2014. *After graduation:* ***Linera*** *(R&D Engineer), Ankara, Turkey*
Thesis Title: "Performance Analysis of Implementation of Radar Signal Processing Algorithms on FPGA and GPU"

13. Mustafa Çavuş, December 2014. *After graduation:* ***University of Rhode Island*** *(PhD Student), Rhode Island, USA*
Currently at: ***Intel*** *(Software Engineer), Hillsboro, Oregon, USA*
Thesis Title: "Online AVF Estimation Using Multi Processing"

14. Osman Seçkin Şimşek, September 2014. *After graduation:* ***University of Manchester*** *(PhD Student), Manchester, Great Britain*
Thesis Title: "OpenCL Based Image Processing Library for Embedded GPGPUs and a Sample Face Detection Application"

15. Hakkı Doğaner Sümerkan, August 2014. *After graduation:* ***University of Notre Dame*** *(PhD Student), Indiana, USA*
Currently at: ***Yugen*** *(Founder), Ankara, Turkey*
Thesis Title: "OpenCL Based Image Processing Library and Kernel Fusion on Embedded Systems"

16. **Abdullah Giray Yağlıkçı**, August 2014. *After graduation:* ***University of Notre Dame*** *(PhD Student), Indiana, USA*
Currently at: ***ETH Zurich*** *(PhD Student), Zurich, Switzerland*
Thesis Title: "Design of an FPGA Based Co-Processor For Digital Signal Processing Applications"
17. **Fahrettin Koç**, August 2013. *After graduation:* ***TÜBITAK SAGE*** *(R&D Engineer), Ankara, Turkey*
Thesis Title: "Content Aware Bitcells Developed to Reduce Static Energy Dissipation for a New SRAM Design: CSRAM"
18. **Mehmet Burak Aykenar**, August 2013. *After graduation:* ***ROKETSAN*** *(R&D Engineer), Ankara, Turkey*
Thesis Title: "FIR Filter Energy and Performance Comparison of GPU and FPGA for Mobile Platforms"
19. **Yaman Çakmakçı**, September 2012. *After graduation:* ***University of Manchester*** *(PhD Student), Manchester, Great Britain*
Currently at: ***OpenSynergy GmbH*** *(Software Engineer), Berlin, Germany*
Thesis Title: "Exploiting Virtual Addresses For Achieving Fault Tolerance In Microprocessors"
20. **Vehbi Eşref Bayraktar**, September 2011. *After graduation:* ***Vivante Corporation*** *(R&D Engineer), Silicon Valley, USA*
Currently at: ***University of California-Davis*** *(PhD Student), California, USA*
Thesis Title: "Tag Simplification : Achieving Power Efficiency Through Reducing The Complexity of the Wake Up Logic"
21. **Görkem Aşılıoğlu**, August 2011. *After graduation:* ***Michigan Technological University*** *(PhD Student), Michigan, USA*
Thesis Title: "Complexity-Effective Rename Table Design For Rapid Speculation Recovery"
Currently at: ***Michigan Technological University*** *(Lecturer), Michigan, USA*
22. **Muhammet Hamdi Yavuz**, September 2010. *After graduation:* ***Infodif*** *(Engineer), Ankara, Turkey*
Currently at: ***Metrc*** *(Chief Software Architect), Florida, USA*
Thesis Title: "Cryptography – Steganography System Design And Implementation Using Music"
23. **Mehmet Kayaalp**, August 2010. *After graduation:* ***Binghamton University****, (PhD Student), New York, USA*
Currently at: ***University of New Hampshire*** *(Assistant Professor), New Hampshire, USA*
Thesis Title: "Protecting The Register File Against Soft Errors Using SRAM Bit Cells With Built-in Comparators"
24. **Yusuf Onur Koçberber**, September 2009. *After graduation:* ***Ecole Polytechnique Federale de Lausenne (EPFL)*** *(PhD Student), Switzerland*
Currently at: ***Oracle Labs*** *(Senior Member of Technical Staff), Zurich, Switzerland*
Thesis Title: "Reducing Static Energy Dissipation of Data Holding Components of Modern Processors"
25. **Meltem Özsoy**, July 2009. *After graduation:* ***Binghamton University*** *(PhD Student), New York, USA*
Currently at: ***Inuitive*** *(Security Software Engineer), Santa Clara, California, USA*
Thesis Title: "Register File Partitioning for Energy Efficiency in Microprocessors"
26. **Hatice Şeyma Ülker**, October 2007. *After graduation:* ***Türk Telekom*** *(Engineer), Ankara, Turkey*
Currently at: ***TÜBİTAK BİLGEM YTE*** *(Chief Expert Researcher), Ankara, Turkey*
Thesis Title: "Hardware design for predicting widths of values produced in microprocessors"
27. **Gülay Yalçın**, September 2007. *After graduation:* ***Barcelona Supercomputing Center*** *(PhD Student), Barcelona, Spain*
Currently at: ***Abdullah Gul University*** *(Assistant Professor), Kayseri, Turkey*
Thesis Title: "Soft Error Detection by Using Tag Comparators in Microprocessors"
28. **Yusuf Sinan Hanay**, June 2007. *After graduation:* ***University of Massachusetts – Amherst*** *(PhD Student), Massachusetts, USA*
Currently at: ***Akdeniz University*** *(Assistant Professor), Antalya, Turkey*
Thesis Title: "Low Power Techniques for Superscalar Microprocessors"
29. **Nisa Bostancı** , expected graduation in 2022. Currently has fellowship offers from Georgia Tech, EPFL and ETH Zürich and trying to decide.
30. **İsmail Emir Yüksel** , ongoing.
31. **Alperen Bolat** , ongoing.
32. **Yahya Can Tuğrul** , ongoing.
33. **Şevval İzmirli** , ongoing.

4.3.5 Undergraduate

- Middle East Technical University, Ankara, Turkey
  1. **Çağrı Eryılmaz**, August 2014. *After graduation:* ***The University of Texas at Austin*** *(PhD Student), Austin, Texas, USA*
  Currently at: ***Intel*** *(SoC Architect), Austin, Texas*
- TOBB University of Economics and Technology, Ankara, Turkey
  2. **Kerem Arıkan,** December 2021. *After graduation:* ***Binghamton University*** *(PhD Student), New York, USA*
  3. **İlker Polat,** August 2020. *After graduation:* ***TU Delft*** *(PhD Student), Amsterdam, Netherlands*
  4. **Volkan Keleş,** April 2016. *After graduation:* ***Apple Inc.*** *(GPU Compiler Engineer), London, Great Britain*
  Senior Project Title: "Energy Aware Big Data Processing Framework"
  5. **Serhat Gesoğlu,** August 2015. *After graduation:* ***University of Manchester*** *(PhD Student), Manchester, Great Britain*
  Senior Project Title: "Exploiting Existing Replicas of Stack Pointer in Register File for Error Detection"
  6. **Begüm Birsen Eğilmez**, April 2014. *After graduation:* ***Northwestern University*** *(PhD Student), Chicago, Illinois, USA*
  Currently at: ***Salesforce*** *(Software Engineer), Washington, USA*
  Senior Project Title: "Accurate Estimation of Smartphone Skin Temperature at Runtime"
  7. **Mustafa Korkmaz**, August 2010. *After graduation:* ***Bilkent University*** *(MS Student), Ankara, Turkey*
  Currently at: ***Google*** *(Software Engineer), Ontario, Canada*
  Senior Project Title: "Employing a General Purpose GPU for Improving the Performance of Regular Workloads"

8. **Zeynep Saka**, August 2010. *After graduation:* ***Bilkent University*** *(MS Student), Ankara, Turkey*
   Currently at: ***University of Waterloo*** *(PhD Student), Ontario, Canada*
   Senior Project Title: "Employing a General Purpose GPU for Improving the Performance of Regular Workloads"
9. **Emine Merve Kaya**, August 2009. *After graduation:* ***Johns Hopkins University*** *(PhD Student), Baltimore, Maryland, USA*
   Currently at: ***X*** *(Research Scientist), San Francisco, California*
   Senior Project Title: "House LP - A 3-Dimensional Social Networking Game"
10. **İlknur Cansu Kaynak**, August 2009. *After graduation:* ***Ecole Polytechnique Federale de Lausenne (EPFL)*** *(PhD Student), Switzerland*
    Currently at: ***Oracle Labs*** *(Senior Member of Technical Staff), Zurich, Switzerland*
    Senior Project Title: "Reducing the Energy Dissipation of the Issue Queue by Exploiting Narrow Immediate Operands"

4.4 Awards

1. **HiPEAC Paper Award**, May 2016.
   HiPEAC, for our paper titled "ChargeCache: Reducing DRAM latency by exploiting row access locality" presented in HPCA 2016.
2. **2009 – 2010 Distinguished Researcher Award**, May 2011.
   TOBB University of Economics and Technology
3. **Second Prize in Conceptual Processor Design Category (Kasırga Processor)**, November 2008.
   "CPU-Turkey" processor design contest
4. **Graduate Student Award for Excellence in Research**, 2005.
   State University of New York at Binghamton
5. **Department of Computer Science Fellowship**, Spring 2003.
   State University of New York at Binghamton

4.5 Technical Presentations

1. "Cloud Computing for Government"
   Turkish Information Technologies Association – 14th Meeting of the Union of Government IT Managers, Belek - Antalya, Turkey, 11 May 2012.
2. "Employing On-Chip Comparator Circuits for Detecting Errors"
   HiPEAC Computing Systems Week, Reliability Task Force Meeting, Wroclaw, Poland, 27 October 2009.
3. "Register Packing: Exploiting Narrow-Width Operands for Reducing Register File Pressure"
   37th International Symposium on Microarchitecture **(MICRO'04)**, Portland, Oregon, USA, 8 December 2004.
4. "Reducing Datapath Energy Through the Isolation of Short-Lived Operands"
   12th International Conference on Parallel Architectures and Compilation Techniques **(PACT'03)**, New Orleans, Louisiana, USA, 1 October 2003.
5. "Reducing Reorder Buffer Complexity Through Selective Operand Caching"
   ACM/IEEE International Symposium on Low Power Electronics and Design **(ISLPED'03)**, Seoul, South Korea, 27 August 2003.
6. "Power Efficient Comparators for Long Arguments in Superscalar Processors"
   ACM/IEEE International Symposium on Low Power Electronics and Design **(ISLPED'03)**, Seoul, South Korea, 26 August 2003.

4.6 Conference Service

- **Program Committee Member**
  - ACM International Conference on Supercomputing (ICS)
    - ICS – 30, May 2016, Istanbul, Turkey
  - IEEE International Conference on Computer Design (ICCD)
    - ICCD – 33, October 2015, New York City, USA
    - ICCD – 32, October 2014, Seoul, South Korea
    - ICCD – 31, October 2013, Asheville, North Carolina, USA
    - ICCD – 30, October 2012, Montreal, Quebec, Canada
    - ICCD – 29, October 2011, Amherst, Massachusetts, USA
    - ICCD – 28, October 2010, Amsterdam, Netherlands
  - IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)
    - DFT – 35, October 2022, Austin, Texas, USA
    - DFT – 34, October 2021, Worldwide Event (due to Covid-19)
    - DFT – 33, October 2020, Rome, Italy
    - DFT – 32, October 2019, Delft, Netherlands
    - DFT – 31, October 2018, Chicago, USA
    - DFT – 30, October 2017, Cambridge, UK
    - DFT – 29, October 2016, Storrs, Connecticut, USA
    - DFT – 28, October 2015, Amherts, Massachusetts, USA
    - DFT – 27, October 2014, Amsterdam, Netherlands
  - IEEE International Conference on High Performance Computing, Data and Analytics (HiPC)
    - HiPC – 23, December 2016, Hyderabad, India
  - Asia Symposium on Quality Electronic Design (ASQED)
    - ASQED – 6, August 2015, Penang, Malaysia
    - ASQED – 5, August 2013, Penang, Malaysia
    - ASQED – 4, July 2012, Penang, Malaysia
    - ASQED – 3, July 2011, Kuala Lumpur, Malaysia
  - Manufacturable and Dependable Multicore Architectures at Nanoscale Workshop (MEDIAN)
    - MEDIAN – Finale, November 2015, Talinn, Estonia
    - MEDIAN – 3, held in conjunction with the Design, Automation and Test in Europe Conference (DATE'14), March 2014, Dresden, Germany
    - MEDIAN – 2, held in conjunction with the IEEE European Testing Symposium (ETS'13), May 2013, Avignon, France
    - MEDIAN – 1, held in conjunction with the IEEE European Testing Symposium (ETS'12), May 2012, Annecy, France

- International Conference on Energy Aware Computing (ICEAC)
  - ICEAC – 5, March 2015, Cairo, Egypt
  - ICEAC – 4, December 2013, Istanbul, Turkey
  - ICEAC – 3, December 2012, Northern Cyprus
  - ICEAC – 2, December 2011, Istanbul, Turkey, (Publication Chair)
- Joint Euro-TM/MEDIAN Workshop on Dependable Multicore and Transactional Memory Systems (DMTM) [to be held in conjunction with the (HiPEAC'14) conference], January 2014, Vienna, Austuria
- HiPEAC Workshop on Design for Reliability (DFR)
  - DFR – 5, held in conjunction with the (HiPEAC'13), January 2013, Berlin, Germany
  - DFR – 4, held in conjunction with the (HiPEAC'12), January 2012, Paris, France
  - DFR – 3, held in conjunction with the (HiPEAC'11), January 2011, Heraklion, Crete, Greece
  - DFR – 2, held in conjunction with the (HiPEAC'10), January 2010, Pisa, Italy
  - DFR – 1, held in conjunction with the (HiPEAC'09), January 2009, Paphos, Cyprus
- Interdisciplinary Engineering Design Education Conference (IEDEC)
  - IEDEC – 4, March 2014, Santa Clara, California, USA
  - IEDEC – 3, March 2013, Santa Clara, California, USA
- Turkish National Embedded Systems and Applications Symposium (GömSis)
  - GömSis – 4, November 2014, Istanbul
  - GömSis – 3, November 2012, Istanbul
  - GömSis – 2, November 2010, Istanbul
  - GömSis – 1, November 2008, Istanbul
- Signal Processing and Communications Applications Conference (SİU)
  - SİU –22, April 2014, Trabzon, Turkey
- 22. International Symposium on Computer and Information Sciences (ISCIS 2007), November 2007, Ankara
- Workshop on Architectural Support for Gigascale Integration (ASGI'06), Boston, USA [held in conjunction with the International Symposium on Computer Architecture (ISCA - 33)], June 2006

- **Organizing Committee Member**
  - Workshop on Architectural Reliability (later Workshop on Dependable Architectures)
    - (WDA – 3) - [held in conjunction with the International Symposium on Microarchitecture (MICRO - 41)], November 2008
    - (WAR – 2) - [held in conjunction with the International Symposium on Microarchitecture (MICRO - 39)], November 2006, Cochairman
    - (WAR – 1) - [held in conjunction with the International Symposium on Microarchitecture (MICRO - 38)], November 2005

4.7 Technical Referee

4.7.1 Research Projects

- Turkish Ministry of Science, Industry and Technology
  - Industrial Thesis Program **(SAN-TEZ)** [2011, 2013]
  - Technological Entrepreneurship Program **(Teknogirişim)** [2012]
  - R&D Centers [2012, 2013]
- The Scientific and Technological Research Council of Turkey (TÜBİTAK)
  - Electrical and Electronics Technology Group Advisory Board Member **(ELOTEG)** [2018, 2019]
  - Technology and Innovation Support Programs **(TEYDEB)** [2008, 2011 – 2022]
  - Electrical, Electronics, Informatics Research Support Programs **(EEEAG)** [2012, 2013, 2017, 2018, 2022]
  - Public Sector Research Grant Committee **(KAMAG)** [2018, 2019]
- European Union (EU)
  - CHISTERA [2014]
- Netherlands Organization for Scientific Research (NWO)
  - Smart Energy Systems Research Program [2010]

4.7.2 Scientific Journals

- ACM Transactions on Architecture and Code Optimization **(TACO)** [2009, 2011, 2013, 2017, 2020, 2021]
- ACM Transactions on Design Automation of Electronic Systems **(TODAES)** [2011, 2015, 2016]
- Computer Applications in Engineering Education **(CAE)** [2010]
- Elsevier Microelectronics Reliability **(MR)** [2015, 2016]
- Elsevier Microprocessors and Microsystems **(MICPRO)** [2013]
- Gazi University Journal of Science **(GUJS)** [2010, 2011]
- IEE Proceedings on Computers and Digital Techniques **(CDT)** [2006]
- IEEE Computer Architecture Letters **(CAL)** [2008, 2015]
- IEEE Transactions on Circuits and Systems I: Regular Papers **(TCAS1)** [2016]
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **(TCAD)** [2011, 2013, 2016, 2017]
- IEEE Transactions on Computers **(TC)** [2004, 2006 – 2015]
  - Special Issue: Defect and Fault Tolerance [2015]
- IEEE Transactions on Device and Materials Reliability **(TDMR)** [2014, 2016, 2018, 2021]
- IEEE Transactions on Emerging Topics in Computing **(TETCSI)** [2016, 2019]
- IEEE Transactions on Industrial Electronics **(TIE)** [2009, 2010]
- IEEE Transactions on Nanotechnology **(TNANO)** [2012]
- IEEE Transactions on Parallel and Distributed Computing **(TPDS)** [2013]
- IEEE Transactions on Reliability [2014]
- IEEE Transactions on Very Large Scale Integration Systems **(TVLSI)** [2014]
- IET Circuits, Devices and Systems **(IET-CDS)** [2013]

- IET Electronics Letters **(IET-ELL)** [2019]
- Journal of Circuits, Systems and Computers **(JCSC)** [2008, 2016]
- Journal of Electronic Testing **(JETT)** [2020]
- Turkish Journal of Electrical Engineering and Computer Sciences **(TJEECS)** [2011, 2012, 2014, 2016, 2019]

4.7.3 Conferences

- European Conference on Circuit Theory and Design **(ECCTD)** [2009]
- Intel Design and Test Technology Conference [Internal Conference] **(Intel DTTC)** [2005]
- International Conference on Computer Design **(ICCD)** [2005, 2006, 2010 – 2013]
- International Conference on High Performance Computing **(HiPC)** [2005]
- International Conference on Parallel Architectures and Compilation Techniques **(PACT)** [2012]
- International Conference on Parallel Processing and Applied Mathematics **(PPAM)** [2013]
- International Conference on Supercomputing **(ICS)** [2014]
- International Symposium on Computer and Information Sciences **(ISCIS)** [2006]
- International Symposium on Computer Architecture **(ISCA)** [2005, 2006, 2010, 2011]
- International Symposium on Microarchitecture **(MICRO)** [2011]
- International Symposium on Performance Analysis of Systems and Software **(ISPASS)** [2006]

5 ACTIVITIES AND MEMBERSHIPS

- Member of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC) (2006 – current)
- Institute of Electrical and Electronics Engineers (IEEE)
  - **Member,** (2011 – 2016)
  - **Student Member,** (2001 – 2005)
  - **Computer Society Member,** (2001 – 2005)
- Association for Computing Machinery (ACM)
  - **Member,** (2015 – 2016)
- Turkish Information Technologies Association – Union of Government IT Managers
  - **Cloud Computing** Work Group, Chairman, 2012
  - **Virtualization** Work Group, Vice Chairman, 2010
- President of the Binghamton University Turkish Student Association (August'01 – March'02), (September'03 – May'04)

6 SKILLS

- Languages: Turkish (Native), English
- Design Tools: Cadence (Virtuoso, Spectre, Affirma), Magic, VHDL, Verilog HDL, HSpice, Microarchitecture Simulators
- Programming: C, C++, Java, Pascal, Haskell